What is claimed is:

1. A data holding device comprising:

a data holding circuit in which data are held by connecting first and second inverter circuits in a loop at the time of latching data; and

a nonvolatile memory element which records a nonvolatile state corresponding to data existing in said data holding circuit with one end of the nonvolatile memory element connected to an input node of said first inverter circuit at the time of writing data, and which discharges an electric charge which corresponds to said nonvolatile state recorded in the nonvolatile memory element and which can generate a voltage higher or lower than the threshold voltage of said first inverter circuit at said input node of said first inverter circuit to said input node of said first inverter circuit when said one end is connected to said input node of said first inverter circuit and a reading signal is applied to the other end of the nonvolatile memory element at the time of restoring data,

said data holding circuit having a loop switching gate which is interposed between a nonvolatile memory element connecting node defined as a connecting node between said input node of said first inverter circuit and said one end of said nonvolatile memory element, and an output node of said second inverter circuit, and which is on at the time of latching and writing data, and off in applying said reading signal and on after a lapse of a predetermined period of time at the time of restoring data.

2. The data holding device as recited in Claim 1, further comprising a data switching gate which has an end connected to said nonvolatile memory element connecting node and the other end connected to a data transmitting path connecting said data holding circuit and the outside, and which is on at the time of transmitting data, and off while said loop switching gate is off and on after a lapse of a predetermined period of time at the time of restoring data.

3. The data holding device as recited in Claim 1, further comprising a limiter element having a connecting-node-side semiconductor region connected to said nonvolatile memory element connecting node, a base semiconductor region to which is applied a power source voltage having a polarity which is the same as that of an electric charge discharged to said nonvolatile memory element connecting node by application of said reading signal, and a junction at which said connecting-node-side semiconductor region is joined to said base semiconductor region in the forward direction for said discharged electric charge.

4. The data holding device as recited in Claim 3,

wherein said loop switching gate and/or said data switching gate have a limiter field-effect transistor as said limiter element,

said limiter field-effect element transistor having a

source/drain region as said connecting-node-side semiconductor region connected to said nonvolatile memory element connecting node, a base semiconductor region to which is applied a power source voltage having a polarity which is the same as that of said electric charge discharged to said nonvolatile memory element connecting node by application of said reading signal, and a junction at which said source/drain region is joined to said base semiconductor region in the forward direction for said discharged electric charge.

5. The data holding device as recited in Claim 1, further comprising a precharge circuit for discharging an electric charge in said non volatile memory element connecting node prior to said application of said reading signal.

6. The data holding device as recited in Claim 5,

wherein said nonvolatile memory element connecting node is connected to an input-side data transmitting path of data transmitting paths connecting said data holding circuit and the outside, and

wherein one correcting inverter circuit is interposed in each of said input-side data transmitting path and an output-side data transmitting path.

7. The data holding device as recited in Claim 1,

wherein said nonvolatile memory element includes a ferroelectric capacitor, and

wherein said nonvolatile state is the polarization state of said ferroelectric capacitor.

8. A data holding method comprising:

a step of preparing a data holding device having a data holding circuit in which data are held by connecting first and second inverter circuits in a loop at the time of latching data, and a nonvolatile memory element having an end which is connected to an input node of said first inverter circuit at least at the time of writing and restoring data,

said data holding circuit having a loop switching gate interposed between a nonvolatile memory element connecting node defined as a connecting node between said input node of said first inverter circuit and said one end of said nonvolatile memory element, and an output node of said second inverter circuit;

a step of recording a nonvolatile state corresponding to data existing in said data holding circuit in said nonvolatile memory element with said one end of said nonvolatile memory element connected to said input node of said first inverter circuit at the time of writing data; and

a step of restoring data corresponding to a nonvolatile state recorded in said nonvolatile memory element in said data holding circuit, including the steps of switching off said loop switching gate with the power source of said data holding device on, allowing said nonvolatile memory element to discharge an electric charge which corresponds to said nonvolatile state

recorded therein and can generate a voltage higher or lower than the threshold voltage of said first inverter circuit at said input node of said first inverter circuit to said input node of said first inverter circuit by connecting said one end of said nonvolatile memory element to said input node of said first inverter circuit and applying a reading signal to the other end of said nonvolatile memory element, and connecting said first and second inverter circuits in a loop by switching on said loop switching gate after a lapse of a predetermined period of time at the time of restoring data.

9. The data holding method as recited in Claim 8,

wherein said data holding device has a data switching gate which has one end connected to said nonvolatile memory element connecting node and the other end connected to a data transmitting path connecting said data holding circuit and the outside, and which is on at the time of transmitting data, and

wherein said step of restoring data corresponding to a nonvolatile state recorded in said nonvolatile memory element in said data holding circuit includes the steps of switching off said loop switching gate and said data switching gate with the power source of said data holding device on, allowing said nonvolatile memory element to discharge an electric charge which corresponds to said nonvolatile state recorded therein and can generate a voltage higher or lower than the threshold voltage of said first inverter circuit at said input node of said first inverter circuit to said input node of said first

inverter circuit by connecting said one end of said nonvolatile memory element to said input node of said first inverter circuit and applying a reading signal to the other end of said nonvolatile memory element, connecting said first and second inverter circuits in a loop by switching on said loop switching gate with said data switching gate kept off after a lapse of a predetermined period of time, and switching on said data switching gate at the time of restoring data.

10. The data holding method as recited in Claim 8,

wherein said nonvolatile memory element includes a ferroelectric capacitor, and

wherein said nonvolatile state is the polarization state of said ferroelectric capacitor.

11. A data holding device having a data holding circuit in which data are held by connecting two inverter circuits in a loop, comprising:

a variable resistance element interposed between a memory node of said data holding circuit and a reference potential; and

a nonvolatile memory element for controlling the resistance value of said variable resistance element,

wherein a state corresponding to data stored in said data holding circuit is recorded in said nonvolatile memory element, and data corresponding to a state recorded in said nonvolatile memory element are restored in said data holding circuit.

12. The data holding device as recited in Claim 11, having two memory nodes, variable resistance elements interposed between said memory nodes and said reference potential, and nonvolatile memory elements provided for said variable resistance elements, respectively, for controlling the resistance values thereof.

13. The data holding device as recited in Claim 11, having two memory node, a variable resistance element interposed between one of said memory nodes and said reference potential, a nonvolatile memory element for controlling the resistance value of said variable resistance element, and a resistance element interposed between the other memory node and said reference potential and having a resistance value within the resistance value of said variable resistance element.

14. The data holding device as recited in Claim 12,

wherein said variable resistance elements are field-effect transistors, and said nonvolatile memory elements are ferroelectric capacitors, and

wherein each of said field-effect transistors has a drain and a source, either of which is connected to one of said memory nodes, and a gate electrode connected to an electrode of one of said ferroelectric capacitors, and a polarization state corresponding to data held in said data holding circuit is recorded in said ferroelectric capacitors by applying a potential of the other memory node to the other electrodes of said ferroelectric capacitors.

15. The data holding device as recited in Claim 13,

wherein said variable resistance element is a field-effect transistor, and said nonvolatile memory element is a ferroelectric capacitor,

said field-effect transistor having a drain and a source, either of which is connected to one of said memory nodes, and a gate electrode connected to one electrode of said ferroelectric capacitor, and a polarization state corresponding to data held in said data holding circuit is recorded in said ferroelectric capacitor by applying a potential of the other memory node to the other electrode of said ferroelectric capacitor.

16. The data holding device as recited in Claim 14, further comprising capacitors connected between said one of memory nodes and said gate electrode.

17. The data holding device as recited in Claim 15, further comprising a capacitor connected between said one of memory nodes and said gate electrode.

18. A data holding device having a data holding circuit in which data are held by connecting two inverter circuits in a loop, comprising:

a variable resistance element interposed between a memory node of said data holding circuit and a reference potential; and

a nonvolatile memory element for controlling the resistance value of said variable resistance element,

wherein a state corresponding to data at optional point in time stored in said data holding circuit is recorded in said nonvolatile memory element and data corresponding to a state recorded in said nonvolatile memory element is restored in said data holding circuit.

19. The data holding device as recited in Claim 18,

wherein said variable resistance element is a field-effect transistor, and said nonvolatile memory element is a ferroelectric capacitor,

wherein said field-effect transistor has a drain and a source, either of which is connected to said memory node, and a gate electrode connected to one of the electrodes of said ferroelectric capacitor, and,

wherein a polarization state corresponding to data at an optional point in time held in said data holding circuit is recorded in said ferroelectric capacitor by applying a nonvolatile memory element writing signal to the other electrode of said ferroelectric capacitor.

20. The data holding device as recited in Claim 19, having two memory nodes,

wherein said drain or source of said field-effect transistor is connected to one of said memory nodes, and

wherein said electrode of said ferroelectric capacitor to

which a nonvolatile memory element writing signal is applied is connected to the other memory node via a nonvolatile memory element writing transistor.

21. A data holding method comprising:

a step of preparing a data holding device having a data holding circuit in which data are held by connecting two inverter circuits in a loop, a variable resistance element interposed between a memory node of said data holding circuit and a reference potential, and a nonvolatile memory element for controlling the resistance value of said variable resistance element;

a step of automatically writing data in said data holding circuit into said nonvolatile memory element;

a step in which said nonvolatile memory element holds the final data in said data holding circuit while the power source of said data holding device is off; and

a step of restoring data held in said nonvolatile memory element in said data holding circuit when said power source of said data holding device is restored.

22. A data holding method comprising:

a step of preparing a data holding device having a data holding circuit in which data are held by connecting two inverter circuits in a loop, a variable resistance element interposed between a memory node of said data holding circuit and a reference potential, and a nonvolatile memory element for

controlling the resistance value of said variable resistance element;

a step of writing data, at an optional point in time, in said data holding circuit into said nonvolatile memory element;

a step in which said nonvolatile memory element holds data written therein while the power source of said data holding device is off; and

a step of restoring data held in said nonvolatile memory element in said data holding circuit when said power source of said data holding device is restored.